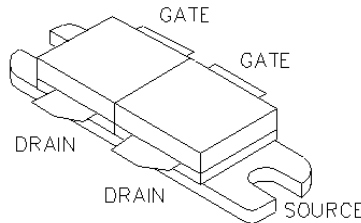




General Description

Silicon VDMOS and LDMOS transistors designed specifically for broadband RF applications. Suitable for Military Radios, Cellular and Paging Amplifier Base Stations, Broadcast FM/AM, MRI, Laser Driver and others.

"Polyfet"TM process features gold metal for greatly extended lifetime. Low output capacitance and high F_t enhance broadband performance



PATENTED GOLD METALIZED SILICON GATE ENHANCEMENT MODE RF POWER VDMOS TRANSISTOR

300 Watts Gemini

Package Style AR

HIGH EFFICIENCY, LINEAR, HIGH GAIN, LOW NOISE

ABSOLUTE MAXIMUM RATINGS (TC = 25 °C)

Total Device Dissipation	Junction to Case Thermal Resistance	Maximum Junction Temperature	Storage Temperature	DC Drain Current	Drain to Gate Voltage	Drain to Source Voltage	Gate to Source Voltage
500 Watts	0.35 °C/W	200 °C	-65 °C to 150 °C	36 A	70 V	70V	30V

RF CHARACTERISTICS (300 WATTS OUTPUT)

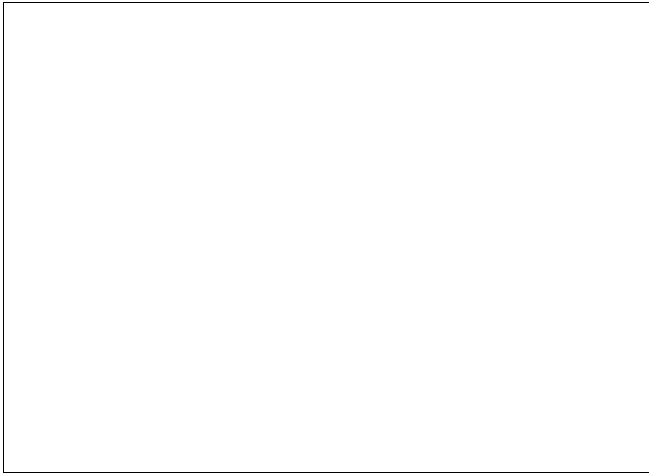
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Gps	Common Source Power Gain	12			dB	$I_{dq} = 4 A, V_{ds} = 28.0V, F = 100 MHz$
η	Drain Efficiency		60		%	$I_{dq} = 4 A, V_{ds} = 28.0V, F = 100 MHz$
VSWR	Load Mismatch Tolerance			20:1	Relative	$I_{dq} = 4 A, V_{ds} = 28.0V, F = 100 MHz$

ELECTRICAL CHARACTERISTICS (EACH SIDE)

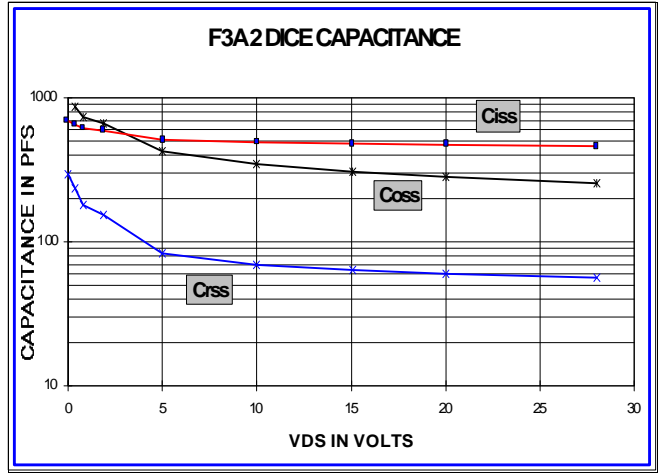
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Bvdss	Drain Breakdown Voltage	65			V	$I_{ds} = 0.2 A, V_{gs} = 0V$
Idss	Zero Bias Drain Current			12	mA	$V_{ds} = 28.0V, V_{gs} = 0V$
Igss	Gate Leakage Current			1	uA	$V_{ds} = 0 V, V_{gs} = 30V$
Vgs	Gate Bias for Drain Current	1		7	V	$I_{ds} = 0.6 A, V_{gs} = V_{ds}$
gM	Forward Transconductance		7		Mho	$V_{ds} = 10V, V_{gs} = 5V$
Rdson	Saturation Resistance		0.1		Ohm	$V_{gs} = 20V, I_{ds} = 20A$
Idsat	Saturation Current		50		Amp	$V_{gs} = 20V, V_{ds} = 10V$
Ciss	Common Source Input Capacitance		400		pF	$V_{ds} = 28.0 V, V_{gs} = 0V, F = 1 MHz$
Crss	Common Source Feedback Capacitance		40		pF	$V_{ds} = 28.0 V, V_{gs} = 0V, F = 1 MHz$
Coss	Common Source Output Capacitance		240		pF	$V_{ds} = 28.0 V, V_{gs} = 0V, F = 1 MHz$

F3002

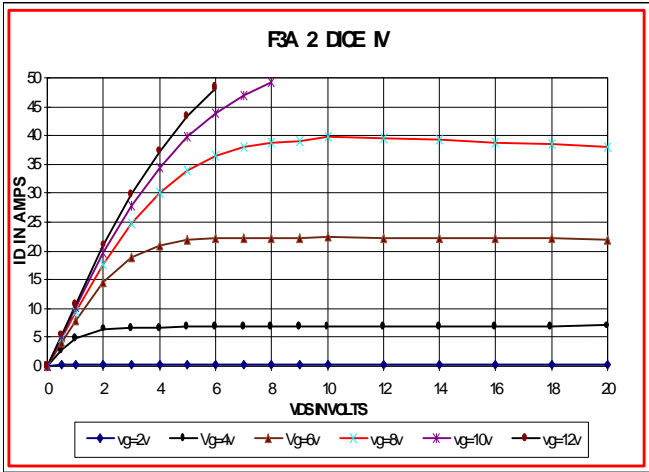
POUT VS PIN GRAPH



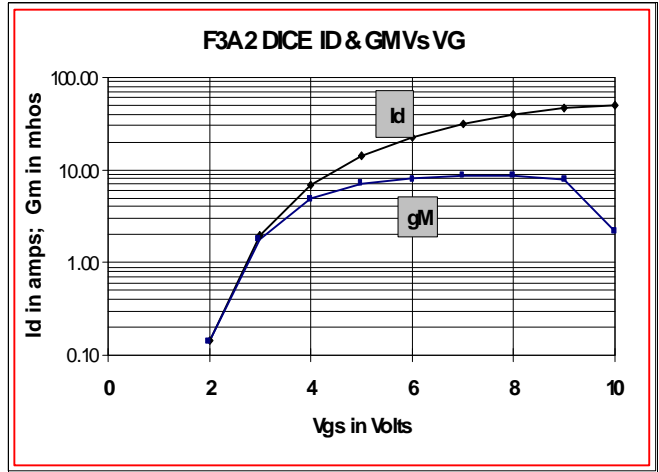
CAPACITANCE VS VOLTAGE



IV CURVE



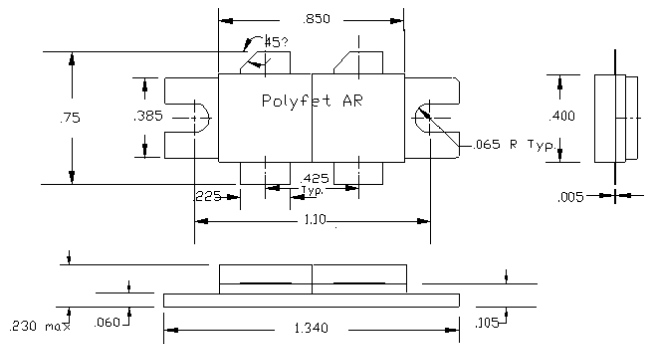
ID AND GM VS VGS



S11 AND S22 SMITH CHART



PACKAGE DIMENSIONS IN INCHES



Polyfet AR Package

Tolerance 0.XX +/- 0.01 0.XXX +/- 0.005 inches

POLYFET RF DEVICES

REVISION 1/12/98