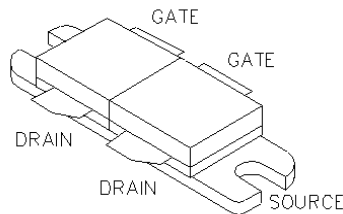




**General Description**

Silicon VDMOS and LDMOS transistors designed specifically for broadband RF applications. Suitable for Military Radios, Cellular and Paging Amplifier Base Stations, Broadcast FM/AM, MRI, Laser Driver and others.

"Polyfet"<sup>TM</sup> process features low feedback and output capacitances, resulting in high  $F_T$  transistors with high input impedance and high efficiency.



**SILICON GATE ENHANCEMENT MODE**

**RF POWER LDMOS TRANSISTOR**

**600.0 Watts Push - Pull**

**Package Style AY**

**HIGH EFFICIENCY, LINEAR**

**HIGH GAIN, LOW NOISE**

**ROHS COMPLIANT**

**ABSOLUTE MAXIMUM RATINGS ( T = 25 °C )**

Total Device Dissipation	Junction to Case Thermal Resistance	Maximum Junction Temperature	Storage Temperature	DC Drain Current	Drain to Gate Voltage	Drain to Source Voltage	Gate to Source Voltage
1,000 Watts	0.18 °C/W	200 °C	-65 °C to 150 °C	24.0 A	110 V	110 V	20 V

**RF CHARACTERISTICS ( 600.0 WATTS OUTPUT )**

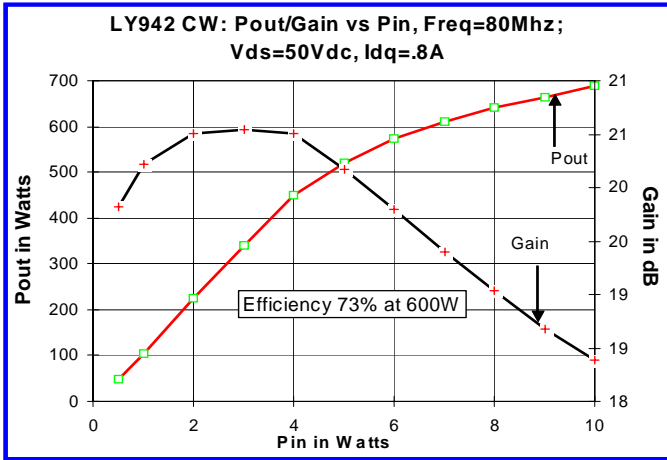
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Gps	Common Source Power Gain	19			dB	Idq = 0.80 A, Vds = 50.0 V, F = 80 MHz
$\eta$	Drain Efficiency		70		%	Idq = 0.80 A, Vds = 50.0 V, F = 80 MHz
VSWR	Load Mismatch Tolerance			13:1	Relative	Idq = 0.80 A, Vds = 50.0 V, F = 80 MHz

**ELECTRICAL CHARACTERISTICS ( EACH SIDE )**

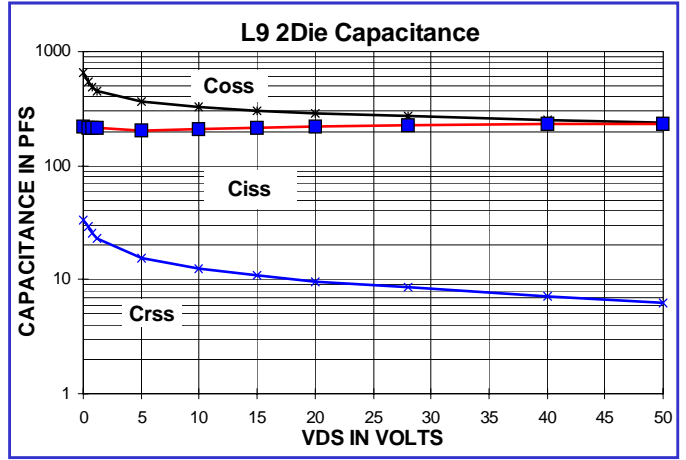
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Bvdss	Drain Breakdown Voltage	110			V	Ids = 100.00 mA, Vgs = 0V
Idss	Zero Bias Drain Current			2.0	mA	Vds = 50.0 V, Vgs = 0V
Igss	Gate Leakage Current			1	uA	Vds = 0V Vgs = 30V
Vgs	Gate Bias for Drain Current	2		5	V	Ids = 0.60 A, Vgs = Vds
gM	Forward Transconductance		7.0		Mho	Vds = 10V, Vgs = 5V
Rdson	Saturation Resistance		0.20		Ohm	Vgs = 20V, Ids = 42.00 A
Idsat	Saturation Current		48.00		Amp	Vgs = 20V, Vds = 10V
Ciss	Common Source Input Capacitance		240.0		pF	Vds = 50.0 Vgs = 0V, F = 1 MHz
Crss	Common Source Feedback Capacitance		7.0		pF	Vds = 50.0 Vgs = 0V, F = 1 MHz
Coss	Common Source Output Capacitance		230.0		pF	Vds = 50.0 Vgs = 0V, F = 1 MHz

# LY942

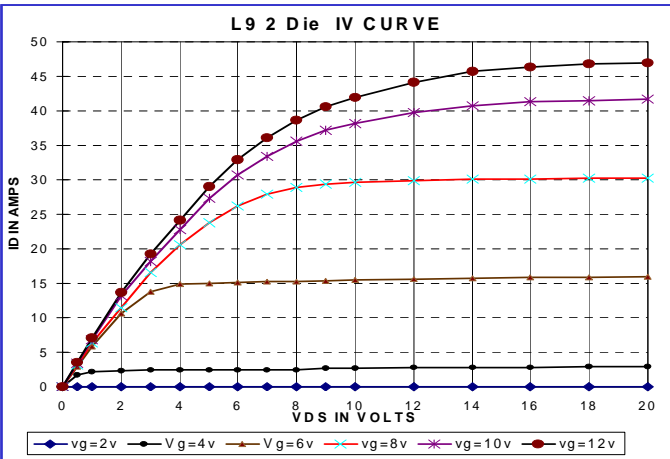
POUT VS PIN GRAPH



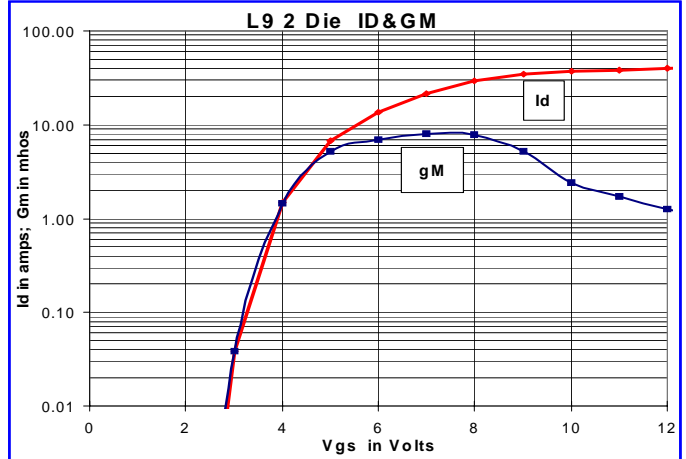
CAPACITANCE VS VOLTAGE



IV CURVE

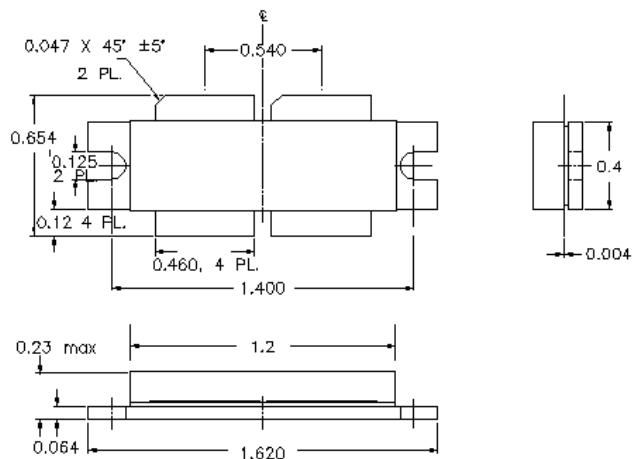


ID & GM VS VGS



Zin Zout

PACKAGE DIMENSIONS IN INCHES



Polyfet AY Package  
Tolerance .XX +/-0.01 .XXX +/-0.005 inches